HMAC SCA Readout controller timing and SCA Channel readout sequence for ATLAS CSC ASMII Boards

Sachin Shrirang Junnarkar
BNL
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sachin@bnl.gov
631-344-2197

This document explains the HAMAC SCA readout sequencer timing and Channel Readout sequence for ATLAS CSC ASMII boards.

Table 1 lists the G-Link pinout and the corresponding simulation names used in the figures used in this document. Same set of names are used in the attached simulation files in Hex format.

Table 1: ASMII Receiver G-Link relevant pinout and corresponding simulation name:

Pin #HDM1022	HDMP Pin Name	Simulation Name	ASM2Signal Name
71	D0	T2X0	RD_CLK
70	D1	T2X1	SD
69	D2	T2X2	RD
68	D3	T2X3	G1
67	D4	T2X4	G0
66	D5	WA7	WA7
65	D6	WA6	WA6
60	D7	WA5	WA5
59	D8	WA4	WA4
58	D9	WA3	WA3
57	D10	WA2	WA2
56	D11	WA1	WA1
55	D12	WA0	WA0
54	D13	T2X13	TRIG_DATA
51	D14	T2X14	ADC_CLK
50	D15	T2X15	20MHZCLOCK
35	STRBOUT	40MHzCLK	STRBOUT

SCA control signals listed in table 1 can be divided as Write operation, Clocks and read operation signals. This document discusses the relative phases and timings of these signals with respect to each other. It is assumed that the state machine controlling these signals is synchronizing the incoming asynchronous trigger to a 40MHz CLOCK.

Read and write operations for the HAMAC SCAs are asynchronous. Both the simultaneous and sequential writes and reads are supported.

Write operation:

WCLK speeds can be 20MHz or 40MHz (Jumper selectable on ASM2).

WA (write address) and WCLK phase relationship is shown in figure 1:

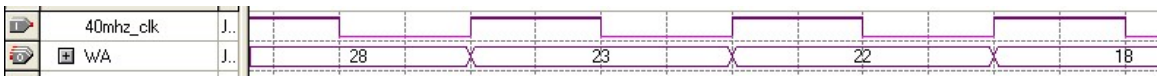

Figure 1:WCLK (40mhz_clk)and WA[7..0]phases

WA[7..0] is rising edge sensitive with respect to 40mhz_clk.

ADC_CLK (T2X14) and SCA RD_CLK (T2X0):

RD_CLK (T2X0) is 25ns phase shifted with respect to ADC_CLK (T2X14), as shown in figure 2.

Figure 2: ADC_CLK (T2X14) and RD_CLK (T2X0) relative phases

Read operation:

All readout signals relative phases are referred to the rising edge of the signal RD (T2X2), although first signal responding to the trigger is SD (T2X1). RD (T2X2) rising edge is marked as 0 in figure 3 and figure 4.

These relationships hold true for both the RD_CLK (T2X0) speeds, 5MHz and 6.66MHz.

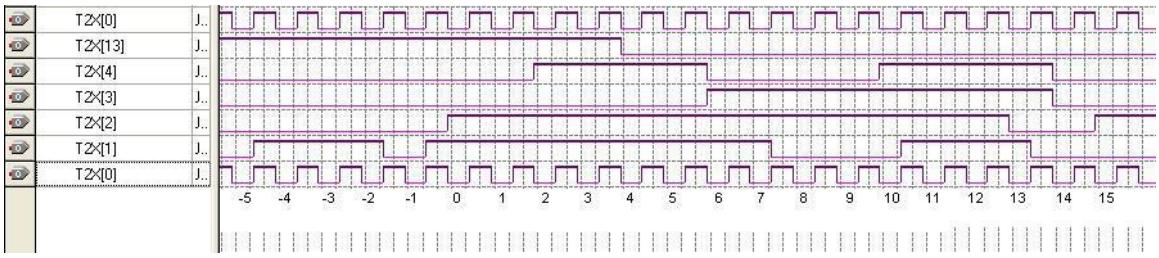

Figure 3: SD (T2X1), RD (T2X2), G0 (T2X4), G1 (T2X3) Timing Diagrams

RD (T2X2), G0 (T2X4) and G1 (T2X3) are **falling** edge sensitive to RD_CLK (T2X0).

RD (T2X2) is high for 12 RD_CLKs and low for 3 RD_CLKs per SCA sample to be readout. (4 samples per trigger in the real experiment)

Valid G0 (T2X4), G1 (T2X3) combinations are sent out 2 falling edges of RD_CLK after 1st RD (T2X2) rising edge. (note activity on T2X3 at clock marked as 2 in figure 3)

G0 (T2X4) is high for 4 RD_CLKs and low for 4 RD_CLKs for the rest of the readout per SCA sample to be readout.

G1 (T2X3) is low for first 4 RD_CLKs. After that G1 (T2X3) is high for 8 RD_CLKS and low for 8 RD_CLKs per SCA sample to be readout for the rest of the readout.

SD (T2X1) is **rising** edge sensitive to RD_CLK (T2X0).

SD (T2X1) is grey coded SCA read address sent out serially, **MSB first**.

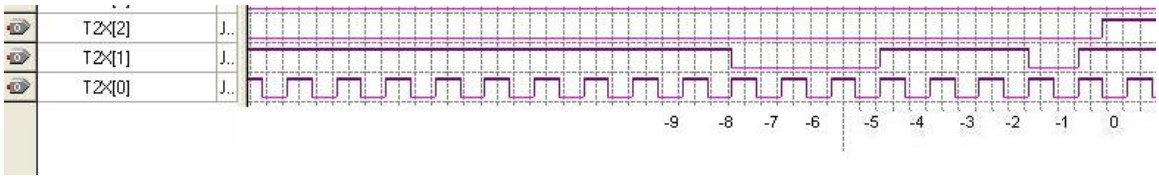

Figure 4: SD (T2X1) goes active 7.5 RD_CLKs (T2X0) before RD (T2X2)

1st SD (T2X1) MSB is sent out 7.5 RD_CLKs, (seen changing at rising edge of RD_CLK (T2X0) marked as -8 in figure 4), before the first RD (T2X2) rising edge (marked as 0 in figure 4).

Finding the start and end of the data stream:

Beginning of the data stream from the ASMII for 2 different RD_CLK speeds is listed below in terms of number of write clocks and number of RD_CLKs from the first rising edge of RD (T2X2). ***Note that changing SCA Write Clock speed to 20MHz from 40MHz doesn't affect numbers in table 2 and table 3.***

Table 2: Start of the data frame with respect to the RD (T2X2) rising edge

	5MHz RD_CLK	**6.66MHz RD_CLK**
TRIG_DATA(T2X13) is ascertained these many #of 40MHzCLKs after 1st rising edge of RD (T2X2)	**38**	**30**

***Table 3:** Width calculation for TRIG_DATA (T2X13)*

	5MHz RD_CLk	6.66 MHz RD_CLK
RD_CLKs period	**200ns**	**150ns**
#of samples in the experiment	**4**	**4**
TRIG_DATA (T2X13) Width in *ns* **=#of Samples*15*RD_CLK period in ns**	**12000ns**	**9000ns**

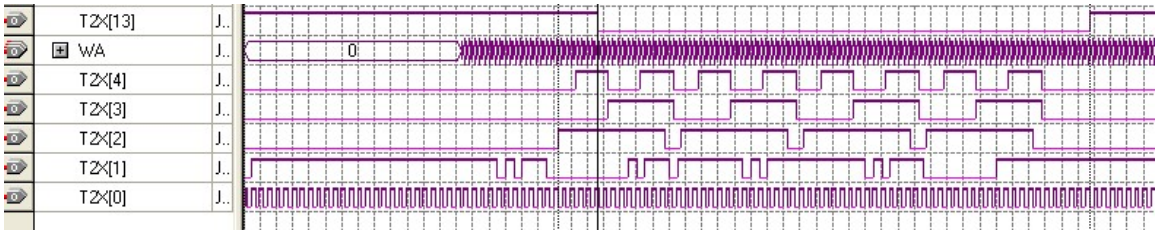

Figure 5: Complete Readout of 4 samples.

Channel ordering and reconstruction:

Data from 2 HAMAC SCAs is multiplexed into 4 G-Link bits at 40MHz. Table 4 gives a map of G-Link nibbles to the corresponding SCA number of origin.

Table 4: ASMII Transmitter G-Link bits mapped to the SCA numbers:

Pin #	HDMP Pin Name	ASM2 name	
59	D0	LINK1_0	SCA1 SCA2
58	D1	LINK1_1	**SCA1 SCA2**
57	D2	LINK1_2	**SCA1 SCA2**
56	D3	LINK1_3	SCA1 SCA2
55	D4	LINK1_4	SCA3 SCA4
54	D5	LINK1_5	**SCA3 SCA4**
53	D6	LINK1_6	**SCA3 SCA4**
51	D7	LINK1_7	SCA3 SCA4
50	D8	LINK1_8	SCA5 SCA6
49	D9	LINK1_9	**SCA5 SCA6**
48	D10	LINK1_10	**SCA5 SCA6**
47	D11	LINK1_11	SCA5 SCA6
46	D12	LINK1_12	SCA7 SCA8
45	D13	LINK1_13	**SCA7 SCA8**
40	D14	LINK1_14	**SCA7 SCA8**
39	D15	LINK1_15	SCA7 SCA8

Unscrambled data from 8 HAMAC SCAs (half ASMII) is ordered for each sample (memory location), as shown in table 5. Note that each sample readout sequence consists of 12 read states and 3 SCA reset states (RD is high for 12 RD_CLKs and low for 3 RD_CLKs). Dummy channels listed in table 5 correspond to the SCA reset states, and SCA outputs are pulled to VREF=2.0V during these 3 states.

Table 5: Channel Readout Order:

LINK1_[3..0]		LINK1_[7..4]		LINK1_[11..8]		LINK1_[15..12]	
DUMMY1-1	**DUMMY2-1**	**DUMMY3-1**	**DUMMY4-1**	**DUMMY5-1**	**DUMMY6-1**	**DUMMY7-1**	**DUMMY8-1**
IN1-1	IN2-1	IN3-1	IN4-1	IN5-1	IN6-1	IN7-1	IN8-1
IN1-2	IN2-2	IN3-2	IN4-2	IN5-2	IN6-2	IN7-2	IN8-2
IN1-3	IN2-3	IN3-3	IN4-3	IN5-3	IN6-3	IN7-3	IN8-3
IN1-4	IN2-4	IN3-4	IN4-4	IN5-4	IN6-4	IN7-4	IN8-4
IN1-5	IN2-5	IN3-5	IN4-5	IN5-5	IN6-5	IN7-5	IN8-5
IN1-6	IN2-6	IN3-6	IN4-6	IN5-6	IN6-6	IN7-6	IN8-6
IN1-7	IN2-7	IN3-7	IN4-7	IN5-7	IN6-7	IN7-7	IN8-7
IN1-8	IN2-8	IN3-8	IN4-8	IN5-8	IN6-8	IN7-8	IN8-8
IN1-9	IN2-9	IN3-9	IN4-9	IN5-9	IN6-9	IN7-9	IN8-9
IN1-10	IN2-10	IN3-10	IN4-10	IN5-10	IN6-10	IN7-10	IN8-10
IN1-11	IN2-11	IN3-11	IN4-11	IN5-11	IN6-11	IN7-11	IN8-11
IN1-12	IN2-12	IN3-12	IN4-12	IN5-12	IN6-12	IN7-12	IN8-12
DUMMY1-2	**DUMMY2-2**	**DUMMY3-2**	**DUMMY4-2**	**DUMMY5-2**	**DUMMY6-2**	**DUMMY7-2**	**DUMMY8-2**
DUMMY1-3	**DUMMY2-3**	**DUMMY3-3**	**DUMMY4-3**	**DUMMY5-3**	**DUMMY6-3**	**DUMMY7-3**	**DUMMY8-3**

Similar table can be written for the readout sequence for the other 8 HAMAC SCAs, sent on LINK2_[15..0]. Those SCA channels are numbered from IN9-[12..1] to IN16-[12..1] and DUMMY9-[3..1] to DUMMY16-[3..1].

Please refer to the ASM2MUX data sheet for reconstructing 12 bit samples from the raw data, knowing the start and the end of the data stream from table 2 and 3.